	Microcontroller and Interfacing (EE 6th Semester) **UNIT 1: Introduction to 8051 Microcontroller**
1	The internal RAM memory of the 8051 is: **A.** 32 bytes **B.** 64 bytes **C.** **128 bytes** **D.** 256 bytes
2	The 8051 has _____ 16-bit counter/timers. **A.** 1 **B.** **2** **C.** 3 **D.** 4
3	The 8051 can handle _____ interrupt sources. **A.** 3 **B.** 4 **C.** **5** **D.** 6
4	When the 8051 is reset and the $\overline{EA}$ line is HIGH, the program counter points to the first program instruction in the: **A.** **internal code memory** **B.** external code memory **C.** internal data memory **D.** external data memory
5	An alternate function of port pin P3.4 in the 8051 is: **A.** **Timer 0** **B.** Timer 1 **C.** interrupt 0 **D.** interrupt 1
6	Microcontrollers often have: **A.** CPUs

	B. RAM **C.** ROM **D.** **all of the above**
7	The total external data memory that can be interfaced to the 8051 is: **A.** 32K **B.** **64K** **C.** 128K **D.** 256K
8	The 8-bit address bus allows access to an address range of: **A.** **0000 to FFFFH** **B.** 000 to FFFH **C.** 00 to FFH **D.** 0 to FH
9	The number of data registers is: **A.** 8 **B.** 16 **C.** **32** **D.** 64
10	When the 8051 is reset and the EA line is LOW, the program counter points to the first program instruction in the: **A.** internal code memory **B.** **external code memory** **C.** internal data memory **D.** external data memory
11	What is the difference between the 8031 and the 8051? **A.** The 8031 has no interrupts. **B.** **The 8031 is ROM-less.** **C.** The 8051 is ROM-less. **D.** The 8051 has 64 bytes more memory.
12	A HIGH on which pin resets the 8051 microcontroller? **A.** RESET

	B. RST **C.** PSEN **D.** RSET
13	An alternate function of port pin P3.1 in the 8051 is: **A.** serial port input **B. serial port output** **C.** memory write strobe **D.** memory read strobe
14	An alternate function of port pin P3.0 (RXD) in the 8051 is: **A. serial port input** **B.** serial port output **C.** memory write strobe **D.** memory read strobe
15	8051 series has how many 16 bit registers? a) **2** b) 3 c) 1 d) 0
16	When 8051 wakes up then 0x00 is loaded to which register? a) DPTR b) SP c) **PC** d) PSW
17	When the microcontroller executes some arithmetic operations, then the flag bits of which register are affected? a) **PSW** b) SP c) DPTR d) PC
18	How are the bits of the register PSW affected if we select Bank2 of 8051? a) PSW.5=0 and PSW.4=1 b) PSW.2=0 and PSW.3=1 c) PSW.3=1 and PSW.4=1 d) **PSW.3=0 and PSW.4=1**
19	If we push data onto the stack then the stack pointer a) **increases with every push** b) decreases with every push c) increases & decreases with every push d) none of the mentioned
20	On power up, the 8051 uses which RAM locations for register R0- R7 a) 00-2F

	b) **00-07** c) 00-7F d) 00-0F
21	The 8051 microcontroller is of ___pin package as a _____ processor. a) 30, 1byte b) 20, 1 byte c) **40, 8 bit** d) 40, 8 byte
22	The SP is of ___ wide register. And this may be defined anywhere in the _____. a) 8 byte, on-chip 128 byte RAM. b) 8 bit, on chip 256 byte RAM. c) 16 bit, on-chip 128 byte ROM d) **8 bit, on chip 128 byte RAM.**
23	After reset, SP register is initialized to address_____. a) 8H b) 9H c) **7H** d) 6H
24	. What is the bit size of the 8051 microcontroller? a) **8-bit** b) 4-bit c) 16-bit d) 32-bit
25	Number of I/O ports in the 8051 microcontroller? a) 3 ports **b) 4 ports** c) 5 ports d) 4 ports with last port having 5 pins
26	Program counter stores what? a) Address of before instruction b) **Address of the next instruction** c) Data of the before execution to be executed d) Data of the execution instruction
27	Auxiliary carry is set during which condition? a) **When carry is generated from D3 to D4** b) When carry is generated from D7 c) When carry is generated from both D3 to D4 and D7 d) When carry is generated at either D3 to D4 or D7
28	What is order of the assembly and running 8051 program? i) Myfile.asm ii) Myfile.lst iii) Myfile.obj iv) Myfile.hex **a) i,ii,iii,iv** b) ii,iii,I,iv c) iv,ii,I,iii d) iii,ii,I,iv
29	Which pin provides a reset option in 8051? a) Pin 1 b) Pin 8 c) Pin 11 **d) Pin 9**
30	External Access is used to permit _____ a) Peripherals b) Power supply c) ALE d) **Memory interfacing**
31	How many interrupts are there in micro controller? a) 3

	b) 6 c) 4 d) **5**
32	**Which register usually store the output generated by ALU in several arithmetic and logical operations?** **a. Accumulator** **b.** Special Function Register **c.** Timer Register **d.** Stack Pointer
33	**How many registers can be utilized to write the programs by an effective selection of register bank in program status word (PSW)?** **a.** 8 **b.** 16 **c. 32** **d.** 64
34	**Which operations are performed by stack pointer during its incremental phase?** **a. Push** **b.** Pop **c.** Return **d.** All of the above
35	**Which is the only register without internal on-chip RAM address in MCS-51?** **a.** Stack Pointer **b. Program Counter** **c.** Data Pointer **d.** Timer Register
36	**Which bit/s play/s a significant role in the selection of a bank register of Program Status Word (PSW)?** **a.** RS1 **b.** RS0 **c. Both a & b** **d.** None of the above
37	**Which flags represent the least significant bit (LSB) and most significant bit (MSB) of Program Status Word (PSW) respectively?** **a. Parity Flag & Carry Flag** **b.** Parity Flag & Auxiliary Carry Flag **c.** Carry Flag & Overflow Flag **d.** Carry Flag & Auxiliary Carry Flag
38	**Which register bank is supposed to get selected if the values of register bank select bits RS1 & Rs0 are detected to be '1' & '0' respectively?** **a.** Bank 0 **b. Bank 1** **c.** Bank 2 **d.** Bank 3
39	**What is the maximum capability of addressing the off-chip data memory & off-chip program memory in a data pointer?** **a.** 8K **b.** 16K **c.** 32K **d. 64K**

40	**Which among the below mentioned functions does not belong to the category of alternate functions usually performed by Port 3 (Pins 10-17)?** **a.** External Interrupts **b. Internal Interrupts** **c.** Serial Ports **d.** Read / Write Control signals
41	A microcontroller at-least should consist of: a) RAM, ROM, I/O devices, serial and parallel ports and timers b) CPU, RAM, I/O devices, serial and parallel ports and timers c) **CPU, RAM, ROM, I/O devices, serial and parallel ports and timers** d) CPU, ROM, I/O devices and timers
42	Unlike microprocessors, microcontrollers make use of batteries because they have: a) high power dissipation b) **low power consumption** c) low voltage consumption d) low current consumption
43	How are microcontrollers classified on the basis of internal bus width? a) 8,16,32,64 bits b) **4,8,16,32 bits** c) 8,16 bits d) 4,16,32 bits
44	Give the names of the buses present in a controller for transferring data from one place to another? a) data bus, address bus b) data bus c) **data bus, address bus, control bus** d) address bus
45	What is the file extension that is loaded in a microcontroller for executing any instruction? a) .doc b) .c c) .txt d) **.hex**
46	What is the most appropriate criterion for choosing the right microcontroller of our choice? a) speed b) availability c) ease with the product d) **all of the mentioned**
47	Why microcontrollers are not called general purpose devices? a) because they are based on VLSI technology b) **because they are not meant to do a single work at a time** c) because they are cheap d) because they consume low power
48	The CF is known as **a) Carry flag** b) Conditional flag c) Common flag **d)** Signal flag

49	Which of the following function relate to stack? a) **Push and pop** b) Call and return c) Both push pop and call return d) None of the mentioned
50	The SF called as a) Single flag **b) Sign flag** c) Super flag d) Service flag

	UNIT 2: Instructions & Programming
1	The contents of the accumulator after this operation MOV A,#0BH ANL A,#2CH will be **A.** 11010111 **B.** 11011010 **C. 00001000** **D.** 00101000
2	Which of the following statements will add the accumulator and register 3? **A.** ADD @R3, @A **B.** ADD @A, R3 **C.** ADD R3, A **D. ADD A, R3**
3	The contents of the accumulator after this operation MOV A,#2BH ORL A,00H will be: **A.** 1B H **B. 2B H** **C.** 3B H **D.** 4B H

4	How are the status of the carry, auxiliary carry and parity flag affected if the write instruction
	MOV A,#9C
	ADD A,#64H
	a) CY=0,AC=0,P=0
	b) CY=1,AC=1,P=0

	c) CY=0,AC=1,P=0 d) CY=1,AC=1,P=1
5	Which of the following is not an instruction of 8051 instructions? a) arithmetic instructions b) boolean instructions c) logical instructions d) **none**
6	The operations performed by data transfer instructions are on a) bit data b) byte data c) 16-bit data d) **all of the mentioned**
7	Which of the following is true while executing data transfer instructions? a) program counter is not accessible b) restricted bit-transfer operations are allowed c) **both operands can be direct/indirect register operands** d) all of the mentioned
8	The logical instruction that affects the carry flag during its execution is a) XRL A; b) ANL A; c) ORL A; d) **RLC A;**
9	All conditional jumps are a) absolute jumps b) long jumps c) **short jumps** d) none
10	The first byte of a short jump instruction represents a) **opcode byte** b) relative address c) opcode field d) none
11	When we add two numbers the destination address must always be. a) some immediate data b) any register c) **accumulator** d) memory
12	If SUBB A,R4 is executed, then actually what operation is being applied? a) R4+A b) R4-A **c) A-R4** d) R4+A
13	A valid division instruction always makes: a) CY=0,AC=1 b) CY=1,AC=1 **c) CY=0,AC=0** d) no relation with AC and CY
14	In 8 bit signed number operations, OV flag is set to 1 if: a) a carry is generated from D7 bit b) a carry is generated from D3 bit

	c) a carry is generated from D7 or D3 bit d) **a carry is generated from D7 or D6 bit**
15	. In unsigned number addition, the status of which bit is important? a) OV b) **CY** c) AC d) PSW
16	Which instructions have no effect on the flags of PSW? a) ANL b) ORL c) XRL d) **All of the mentioned**
17	ANL instruction is used _____ a) to AND the contents of the two registers b) to mask the status of the bits c) **all of the mentioned** d) none of the mentioned
18	CJNE instruction makes _____ a) the pointer to jump if the values of the destination and the source address are equal b) sets CY=1, if the contents of the destination register are greater then that of the source register c) sets CY=0, if the contents of the destination register are smaller then that of the source register d) **none of the mentioned**
19	XRL, ORL, ANL commands have _____ a) **accumulator as the destination address and any register, memory or any immediate data as the source address** b) accumulator as the destination address and any immediate data as the source address c) any register as the destination address and accumulator, memory or any immediate data as the source address d) any register as the destination address and any immediate data as the source address
20	**Which general purpose register holds eight bit divisor and store the remainder especially after the execution of division operation?** **a.** A-Register **b. B-Register** **c.** Registers R0 through R7 **d.** All of the above
21	**What kind of instructions usually affect the program counter?** **a.** Call & Jump **b. Call & Return** **c.** Push & Pop **d.** Return & Jump
22	**It is possible to set the auxiliary carry flag while performing addition or subtraction operations only when the carry exceeds _____** **a.** 1st bit **b.** 2nd bit

	c. 3rd bit **d.** 4th bit
23	DJNZ R0, label is how many bit instructions? a) **2** b) 3 c) 1 d) Can't be determined
24	JZ, JNZ, DJNZ, JC, JNC instructions monitor the bits of which register? a) DPTR b) B c) A d) **PSW**
25	When the call instruction is executed the topmost element of stack comes out to be a) the address where stack pointer starts b) **the address next to the call instruction** c) address of the call instruction d) next address of the stack pointer
26	LCALL instruction takes a) 2 bytes b) 4 bytes c) **3 bytes** d) 1 byte
27	Are PUSH and POP instructions are a type of CALL instructions? a) yes b) **no** c) none of the mentioned d) cant be determined
28	What is the time taken by one machine cycle if crystal frequency is 20MHz? a) 1.085 micro seconds b) **0.60 micro seconds** c) 0.75 micro seconds d) 1 micro seconds
29	What is the time taken by one machine cycle if crystal frequency is 11.0596MHz? a) **1.085 micro seconds** b) 0.60 micro seconds c) 0.75 micro seconds d) 1 micro seconds
30	The last statement of the source program should be _____ • **A.** Stop • **B.** Return • **C.** OPcode • **D. End**
31	If ADD A,R4 is executed, then actually what operation is being applied? **a) A+R4** b) R4-A c) A-R4 d) none of above
32	Which of the following is correct about the MUL instruction? a. it is a byte-by- byte multiplication instruction b. the product is stored in two registers R1 and R0

	c. **both of the mentioned** d. none of the mentioned
33	A valid division instruction always makes: a. CY=0,AC=1 b. CY=1,AC=1 **c. CY=0,AC=0** d. no relation with AC and CY
34	**Which among the category of program branching instructions allow 16 bit address to be specified & can jump anywhere within 64K block of program memory?** **a. Long jumps (LJMP)** **b.** Short jumps (SJMP) **c.** Absolute jumps (AJMP) **d.** All of the above
35	**What is the possible range of transfer control for 8-bit relative address especially in 2's complement form with respect to the first byte of preceding instruction?** **a.** -115 to 132 bytes **b.** -130 to 132 bytes **c. -128 to 127 bytes** **d.** -115 to 127 bytes
36	**Which rotate instruction has an ability to modify CY flag by moving the bit-7 to bit-0 to an accumulator?** a. RR b. **RLC** c. RRC d. RL
37	**Which rotate instruction has an ability to modify CY flag by moving the bit-0 to bit-7 to an accumulator?** a. RR b. RLC c. **RRC** d. RL
38	**Which rotate instruction has an ability to moving the bit-7 to bit-0 to an accumulator?** a. RR b. RLC c. RRC d. **RL**
39	**Which rotate instruction has an ability to moving the bit-0 to bit-7 to an accumulator?** a. **RR** b. RLC c. RRC d. RL
40	**Which among the single operand instructions complement the accumulator without affecting any of the flags?** a. CLR b. SETB

	c. **CPL** d. All of the above
41	Which of the following is not a data copy/transfer instruction? **a) MOV** b) PUSH c) JMP d) POP
42	**Which among the single operand instructions clear the accumulator?** a. **CLR** b. SETB c. CPL d. All of the above
43	**Which among the single operand instructions set the bit?** a. CLR b. **SETB** c. CPL d. All of the above
44	What is the instruction to add 55H in an accumulator? a) MOV A,55H b) ADD A,55H c) **ADD A,#55H** d) None of these
45	What is the instruction to sub 55H in an accumulator? a) MOV A,55H b) **SUBB A,#55H** c) ADD A,#55H d) None of these
46	What is the instruction to add the content of 40H in an accumulator? a) MOV A,40H b) **ADD A,40H** c) ADD A,#40H d) None of these
47	Represent -7 in hexadecimal number a) C8H b) **F9H** c) B3H d) 22H
48	Represent -56 in hexadecimal number a) **C8H** b) F9H c) B3H d) 22H
49	What is the time taken by one machine cycle if crystal frequency is 16MHz? a) 1.085 micro seconds b) 0.60 micro seconds c) **0.75 micro seconds** d) 1 micro seconds
50	What is the time taken by one machine cycle if crystal frequency is 22 MHz? a) 1.085 micro seconds b) 0.60 micro seconds

	c) 0.75 micro seconds d) **0.545 micro seconds**

	UNIT 3: Addressing Modes
1	MOV A, @ R1 will: **A.** copy R1 to the accumulator **B.** copy the accumulator to R1 **C.** **copy the contents of memory whose address is in R1 to the accumulator** **D.** copy the accumulator to the contents of memory whose address is in R1
2	The I/O ports that are used as address and data for external memory are: **A.** ports 1 and 2 **B.** ports 1 and 3 **C.** **ports 0 and 2** **D.** ports 0 and 3
3	The 8051 has _____ parallel I/O ports. **A.** 2 **B.** 3 **C.** **4** **D.** 5
4	Bit-addressable memory locations are: **A.** 10H through 1FH **B.** **20H through 2FH** **C.** 30H through 3FH **D.** 40H through 4FH
5	Which of the following instructions will move the contents of register 3 to the accumulator? **A.** MOV 3R, A **B.** MOV R3, A **C.** **MOV A, R3** **D.** MOV A, 3R
6	Which of the following commands will move the number 27H into the accumulator? **A.** MOV A, P27

	B. MOV A, #27H **C.** MOV A, 27H **D.** MOV A, @27
7	Which of the following commands will move the value at port 3 to register 2? **A.** MOV P2, R3 **B.** MOV R3, P2 **C.** MOV 3P, R2 **D. MOV R2, P3**
8	The I/O port that does not have a dual-purpose role is: **A.** port 0 **B. port 1** **C.** port 2 **D.** port 3
9	Which of the following commands will copy the contents of RAM whose address is in register 0 to port 1? **A.** MOV @ P1, R0 **B.** MOV @ R0, P1 **C. MOV P1, @ R0** **D.** MOV P1, R0
10	Which of the following commands will copy the contents of location 4H to the accumulator? **A. MOV A, 04H** **B.** MOV A, L4 **C.** MOV L4, A **D.** MOV 04H, A
11	Which of the following instructions will move the contents of the accumulator to register 6? **A.** MOV 6R, A **B. MOV R6, A** **C.** MOV A, 6R **D.** MOV A, R6

12	How many bytes of bit addressable memory is present in 8051 based microcontrollers? a) 8 bytes b) 32 bytes c) **16 bytes** d) 128 bytes
13	What is the address range of SFR Register bank? a) 00H-77H b) 40H-80H c) 80H-7FH d) **80H-FFH**
14	Which pin of port 3 is has an alternative function as write control signal for external data memory? a) P3.8 b) P3.3 c) **P3.6** d) P3.1
15	To initialize any port as an output port what value is to be given to it? a) 0xFF b) 0x00 c) 0x01 d) **A port is by default an output port**
16	Which out of the four ports of 8051 needs a pull-up resistor for using it is as an input or an output port? a) **PORT 0** b) PORT 1 c) PORT 2 d) PORT 3
17	Which of the ports act as the 16 bit address lines for transferring data through it? a) PORT 0 and PORT 1 b) PORT 1 and PORT 2 c) **PORT 0 and PORT 2** d) PORT 1 and PORT 3
18	Which of the following registers are not bit addressable? a) SCON b) **PCON** c) A d) PSW
19	Which instruction is used to check the status of a single bit? a) MOV A,P0 b) ADD A,#05H c) **JNB PO.0, label** d) CLR P0.05H
20	Which addressing mode is used in pushing or popping any element on or from the stack? a) immediate b) **direct** c) indirect d) register
21	Which operator is the most important while assigning any instruction as register indirect instruction? a) $ b) # **c) @** d) &
22	What is the advantage of register indirect addressing mode? a) it makes use of registers R0 and R1

	b) it uses the data dynamically c) it makes use of operator @ d) it is easy
23	Which of the following comes under the indexed addressing mode? a) MOVX A, @DPTR b) **MOVC @A+DPTR,A** c) MOV A,R0 d) MOV @R0,A
24	Is this a valid statement? SETB A a) yes b) **no** c) cant be determined d) none of the mentioned
25	**Which bits of opcode specify the type of registers to be used in the register addressing mode?** a. **LSB** b. MSB c. both a & b d. none of the above
26	**Which base-register is preferred for address calculation of a byte that is to be accessed from program memory by base-register plus register-indirect addressing mode?** a. **DPTR** b. PSW c. PCON d. All of the above
27	**What does the symbol '#' represent in the instruction MOV A, #55H ?** a. Direct datatype b. Indirect datatype c. **Immediate datatype** d. Indexed datatype
28	Which operations are performed by the bit manipulating instructions of boolean processor? a. Complement bit b. Set bit c. Clear bit **d. All of the above**
29	**Which locations of 128 bytes on-chip additional RAM are generally reserved for special functions?** **a. 80H to 0FFH** **b.** 70H to 0FFH **c.** 90H to 0FFH **d.** 60H to 0FFH
30	**Which commands are used for addressing the off-chip data and associated codes respectively by data pointer?**

	a. MOVX & MOVC **b.** MOVY & MOVB **c.** MOVZ & MOVA **d.** MOVC & MOVY
31	**Which instruction find its utility in loading the data pointer with 16 bits immediate data?** **a. MOV** **b.** INC **c.** DEC **d.** ADDC
32	**Which port does not represent quasi-bidirectional nature of I/O ports in accordance to the pin configuration of 8051 microcontroller?** **a. Port 0 (Pins 32-39)** **b.** Port 1 (Pins 1-8) **c.** Port 2 (Pins 21-28) **d.** Port 3 (Pins 10-17)
33	**The upper 128 bytes of an internal data memory from 80H through FFH usually represent _____.** **a.** general-purpose registers **b. special function registers** **c.** stack pointers **d.** program counters
34	**What is the bit addressing range of addressable individual bits over the on-chip RAM?** **a.** 00H to FFH **b**. 01H to 7FH **c. 00H to 7FH** **d.** 80H to FFH
35	In which of these modes, the immediate operand is included in the instruction itself? a) register operand mode b) **immediate operand mode** c) register and immediate operand mode d) none of the mentioned
36	If the stack flag is set, and condition code bit C1=1, then the stack is a) full b) **overflown** c) underflown d) empty
37	If the stack flag is set, and condition code bit C1=0, then the stack is a) full b) overflown c) **underflown** d) empty
38	What is the meaning of the instruction MOV A,05H? a) data 05H is stored in the accumulator b) fifth bit of accumulator is set to one c) **address 05H is stored in the accumulator** d) none of the mentioned

39	**How does the microcontroller communicate with the external peripherals / memory?** a. **via I/O ports** b. via register arrays c. via memory d. all of the above
40	**Why do the microprocessors possess very few bit manipulating instructions?** a. Because they mostly operate on bits/ word data b. **Because they mostly operate on byte/word data** c. Both a & b d. None of the above
41	The addressing mode which makes use of in-direction pointers is _____ a) **Indirect addressing mode** b) Index addressing mode c) Relative addressing mode d) Offset addressing mode
42	Which of the following instructions will move the contents of accumulator to the register 2? **A.** MOV 2R, A **B. MOV R2, A** **C.** MOV A, R2 **D.** MOV A, 2R
43	What is the address of special function register accumulator? **a) 0E0H** b) 80H c) 89H d) 81H
44	What is the address of special function register accumulator? a) 0E0H **b) 80H** c) 89H d) 81H
45	What is the function of SETB bit? a) Set bit=0 b) Set bit=2 **c) Set bit=1** d) None of above
46	What is the function of CLR bit? a) Clear bit b) Set bit **c)** Both a & b d) None of above
47	SETB 86H=? a) **SETB P0.6** b) SETB P1.7 c) SETB P2.3 d) CLR P 3.2

48	CLR 97H=? a) SETB P0.6 b) **CLR P1.7** c) SETB P2.3 d) CLR P 3.2
49	What is the function of JNB bit, target? a) Jump to target if bit=2 b) Jump to target if bit=1 **c) Jump to target if bit=0** d) None of above
50	What is the function of JB bit, target? a) Jump to target if bit=2 **b) Jump to target if bit=1** c) Jump to target if bit=0 d) None of above